

Claims

[c1] What is claimed is:

1.A method of fabricating a low temperature polysilicon (LTPS) thin film transistor (TFT), the method comprising following steps:
providing a substrate;
forming a polysilicon film on the substrate, the polysilicon film defined with a source region, a drain region, and a channel region between the source region and the drain region;
forming a gate insulating layer on the substrate;
forming a gate on the substrate;
performing an ion implantation process to form a source in the source region and a drain in the drain region;
forming a silicon nitride layer covering the gate and the polysilicon film; and
forming a TEOS based silicon oxide layer on the silicon nitride layer.

[c2] 2.The method of claim 1 further comprising following steps:

performing a photo-etching process to form a contact hole on the source and another contact hole on the

drain; and

filling a conductive layer in the contact holes, the conductive layer being electrically connected to the source and the drain.

- [c3] 3. The method of claim 1 wherein the method of forming the polysilicon film comprises following steps: forming an amorphous silicon film on the substrate; and performing an excimer laser annealing process to make the amorphous silicon film crystallize to the polysilicon film.
- [c4] 4. The method of claim 1 wherein the silicon nitride layer is a silane based silicon nitride layer.
- [c5] 5. The method of claim 4 wherein the silicon nitride layer comprises 20% to 40% hydrogen atoms and serves as a hydrogen source of a hydrogenating process.
- [c6] 6. The method of claim 1 wherein the gate is a metal gate.
- [c7] 7. The method of claim 1 wherein the silicon oxide has a thickness in a range of 2500 to 10000 angstroms.
- [c8] 8. The method of claim 1 wherein the silicon nitride has a thickness in a range of 500 to 3500 angstroms.
- [c9] 9. The method of claim 1 wherein the method forms the

silicon nitride layer by performing a first plasma enhanced chemical vapor deposition (PECVD) process.

- [c10] 10. The method of claim 9 wherein the method forms the silicon oxide layer by performing a second plasma enhanced chemical vapor deposition process.
- [c11] 11. The method of claim 10 wherein the first PECVD process and the second PECVD process are performed in the same reacting chamber.
- [c12] 12. The method of claim 10 wherein the first PECVD process and the second PECVD process are performed in different reacting chambers.
- [c13] 13. The method of claim 1 wherein the low temperature polysilicon thin film transistor is a top gate low temperature polysilicon thin film transistor or a bottom gate low temperature polysilicon thin film transistor.